In the Specification:

Please replace the "Cross Reference To Related Applications" located at page 1, lines 5 to 25 with the following:

Cross Reference to Related Applications:

The following copending applications, assigned to the assignee of the present invention, contain common disclosure and are incorporated herein by reference in their entireties:

"High Speed Software Driven Emulator Comprised of a Plurality of Emulation Processors with Improved Board-to-Board Interconnection Cable Length Identification System," Serial No. 09/655,595, filed September 6, 2000.

"High Speed Software Driven Emulator Comprised of a Plurality of Emulation Processors with an Improved Maintenance Bus that Streams Data at High Speed," Serial No. 09/656,147, filed September 6, 2000.

"High Speed Software Driven Emulator Comprised of a Plurality of Emulation Processors with a Method to Allow High Speed Bulk Read/Write Operation Synchronous DRAM While Refreshing the Memory," Serial No. 09/656,541, filed September 6, 2000.

"High Speed Software Driven Emulator Comprised of a Plurality of Emulation Processors with a Method to Allow Memory Read/Writes Without Interrupting the Emulation," Serial No. 09/656,596, filed September 6, 2000.

Please replace the paragraph on page 4, lines 4-9 with the following:

For purposes of better understanding the structure and operation of emulation devices generally, and this invention particularly, United States Patent Nos. 5,551,013 and 6,618,698 and assigned to the assignee of this application are hereby incorporated herein by reference.

Please replace the paragraph on page 5, line 12 through page 6, line 14 with the following:

Each of these emulation processors has an execution unit for processing multiple types of logic gate functions. Each emulation processor switches from a specified one logic gate function to a next logic gate function in a switched-emulation sequence of different gate functions. The switched-emulation sequence of each of the processors thus can emulate a subset of gates in a hardware arrangement in which gates are of any type that the emulation processors functionality represents for a sequence of clock cycles. The processors are coupled by a like number of multiplexors having outputs respectively connected to the emulation processors of a module and having inputs respectively connected to each of the other emulation processors. The bus connected to the multiplexors enables an output from any emulation processor to be transferred to an input of any other of the emulation processors. In accordance with the teachings of the pending application, this basic design of the 5,551,013 patent is improved by interconnecting processors into clusters. With the processors interconnected in clusters, the evaluation phases can be cascaded, and all processors in a cluster perform the setup and storing of results in parallel. This setup includes routing of the data through multiple evaluation units for the evaluation phase. For most efficient operation, the input stack and data stack of each processor must be stored in shared memory within each cluster. Then, all processors perform the storage phase, again in parallel. The net result is multiple cascaded evaluations performed in a single emulation step. Every processor in a cluster can access the input and data stacks of every other processor in the cluster and the less space on each module chip for the functions that support the processor operation, particularly the memory functions. While the emulation processor described in U.S. Patent No. 6,618,698 has obvious advantages, as more and more components

are placed on a singe ET 4 chip, the availability of real estate on the chip becomes more and more a factor in the successful realization of an advanced emulation processor design.

Please replace the paragraph on page 7, line 21 through page 8, line 11 with the following:

Referring now to Figure 1, as described more completely in U.S. Patent No. 6,618,698, each cluster of four processors (Processor0, Processor1, Processor2 and Processor3) has a shared data and input memory stack to which and from which each processor in the cluster can write and read. In this exemplary emulation processor, the memory stack has 256 addressable eight-bit words. Each processor has four read ports for reading an eight-bit word from the data memory comprised of address inputs RA0; RA1; RA2 and RA3 and corresponding inputs to the four eight-to-one multiplexers whose select inputs are TAC0; TAC1; TAC2 and TAC3 respectively. On each clock cycle, the inputs of the eight-to-one multiplexer of each of the four processors receives an eight-bit word from the memory. While generally satisfactory, there are a large number of processors (e.g. 64) and a correspondingly large number of memory stacks on a single ET 4 emulator chip. Silicon real estate is in short supply and the stack memory output ports take up a lot of area on the chip.